

PTO/SB/08a (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1

of 4

Complete if Known

Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Richard E. Perego
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	RAMB-01049US2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-5,953,215*	09-14-1999	Karabatsos	
		US-6,142,830*	11-07-2000	Looeffler	
		US-6,185,644 B1*	02-06-2001	Farmwald et al.	
		US-6,266,252 B1*	07-24-2001	Karabatsos	
		US-6,317,352 B1*	11-13-2001	Halbert et al.	
		US-6,414,904 B2*	07-02-2002	So et al.	
		US-6,446,158 B1*	09-03-2002	Karabatsos	
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		US-6,530,006 B1*	03-04-2003	Dodd et al.	
		US-6,643,752 B1*	11-04-2003	Donnelly et al.	
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		US-6,108,731*	08-22-2000	Suzuki et al.	
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		US-5,068,650*	11-26-1991	Fernandez et al.	
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		US-6,185,644*	02-06-2001	Farmwald et al.	

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

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Sheet 2

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Sheet 3 of 4

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		*Intel Developer Forum, "DDR2 Memory In 2004 Servers - Recipes For Successful Designs", September 2003	
		*QBM Alliance, Platform Conference, "Quad Band Memory (QBM tm): DDR 200/266/333 devices producing DDR400/533/667, Jan. 23-24, 2002	
		*KARABATSOS, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., April 2001	
		*Quad Band Memory (QBM), "The 'QBM Enabled' VIA PT880/PM880 Chipset Solutions with the Fastest Memory",	
		*WEBER, F., "The AMD Athlon Processor: Future Directions", AMD	
		*"Intel 82804AA Memory Repeater Hub for SDRAM (MRH-S) Datasheet", Intel Corp., pp. 2-48 (Nov. 1999)	
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		*CATALDO, A., "TI Fields DSP-Based Media Processor on a DIMM", EE Times (Jan. 2000)	
		*MAC WILLIAMS, P., "PC Memory Directions For 1999 and Beyond", Intel Developer Forum, pp. 1-10 (Sep. 1998)	
		*JOHNSON, B., "Direct RDRAM Basic Architecture and Program Overview", Intel Developer Forum, pp. 1-14 (Sep. 1998)	

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First Named Inventor

Perego

Art Unit

2188

Examiner Name

Attorney Docket Number

RAMB-01049US2

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		*JONES, F (United Memories, Inc.), "A new era of fast dynamic RAMs", IEEE Spectrum, October 1992, pp. 43-49	
		*FARMWALD, M. et al. (Rambus Inc.), "A fast path to one memory", IEEE Spectrum, October 1992, pp. 50-51	
		*GJESSING, S. (University of Oslo), GUSTAVSON, D.B (Stanford Linear Accelerator Center), JAMES, D. et al. (Apple Computer Inc.), WIGGER, H. (Hewlett-Packard Co.), "A RAM link for high speed", IEEE Spectrum, October 1992, pp. 52-53	
		*The Institute of Electrical and Electronics Engineering, Inc., "IEEE Standard for High-Bandwidth Memory Interface Based on Scalable Coherent Interface (SCI) Signaling Technology (RamLink)", 1996, pp. 1-91	

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Richard E. Perego

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		*GILLINGHAM, P., "SLDRAM Architectural and Functional Overview", SLDRAM Consortium, SLDRAM Inc., pp. 1-14 (Aug. 1997)	
		**Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X, IEEE Inc., pp. 1-51 (1996)	
		*WIGGERS, H., "SyncLink A Proposal for an Implementation of IEEE P1596.4", Hewlett Packard, pp. 1-20 (Mar. 1995)	
		**KMM377S1620CT2 SDRAM Module Datasheet", Samsung Electronics Inc., pp. 1-2 (Nov. 1998)	
		**SLD4M18DR400 4MEG x 18 SLDRAM Datasheet", SLDRAM Inc., pp. 1-69 (July 1998)	
		*POULTON, J., "Signaling in High Performance Memory Systems", IEEE Solid State Circuits Conference, slides 1-59 (Feb. 1999)	
		**SLDRAM 400Mb/s/pin Command/Address Repeater", SLD10400 Rev .5, SLDRAM Consortium, pp. 1-12 (Jan. 7, 1998)	
		*Minutes of meeting no. 75 JEDEC JC-42.3 Committee on RAM Memories, and referenced attachment "Y" of the presentation titled "SyncLink", May 24, 1995, New Orleans	
		*Intel Developer Forum, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity", February 18, 2004	
		*Intel Developer Forum, "Fully Buffered DIMM (FB-DIMM) Design Considerations", February 18, 2004	

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Sheet	1	of	1
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First Named Inventor	Perego
Art Unit	Unknown
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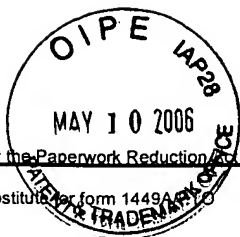
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		US-6690726*	02-10-2004	Yavits et al.	
		US-5325493*	06-28-1994	Herrell et al.	
		US-5867180*	02-02-1999	Katayama et al.	
		US-6104417*	08-15-2000	Nielsen et al.	
		US-6208273*	03-27-2001	Dye et al.	
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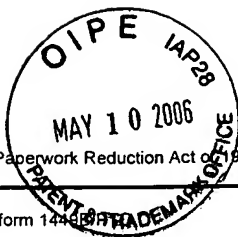
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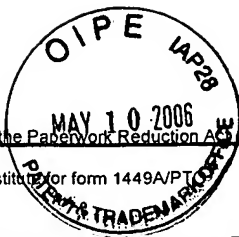
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		*IEEE Standard for Scalable Coherent Interface (SCI), "Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society", IEEE Std 1596-1992	
		*SCI, "P1596: SCI, A Scalable Coherent Interface", November 28, 1988	
		*GUSTAVSON et al., DRAFT "The Scalable Coherent Interface Project (SuperBus)", SCI, August 22, 1988, Rev. 14	
		*SCHANKE, "Proposal for Clock Distribution in SCI", SCI, May 5, 1989	
		*JAMES, "Scalable I/O Architecture for Buses", COMPCON Spring 1989, SCI, November 28, 1988	
		*VOLZ et al., "Position Paper On Global Clock For the Futurebus +", SCI, 1989	
		*KRISTIANSEN et al., "Scalable Coherent Interface", to appear in Eurobus Conference Proceedings, May 1989	

Examiner
SignatureDate
Considered

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1

of 2

Complete if Known

Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Perego
Art Unit	2188
Examiner Name	
Attorney Docket Number	RAMB-01049US2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-			
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 0 811 916 A2*	12/10/1997	The Boeing		
		WO 99/30240*	06-17-1999	Intel Corporation		
		WO 99/41666*	08-19-1999	Intel Corporation		
		WO 99/41667*	08-19-1999	Intel Corporation		
		EP 1069509 A2*	01-17-2001	Texas Instruments Incorporated		

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				Application Number	10/766,131
				Filing Date	January 28, 2004
				First Named Inventor	Perego
				Art Unit	2188
				Examiner Name	
				Attorney Docket Number	RAMB-01049US2
Sheet	2	of	2		

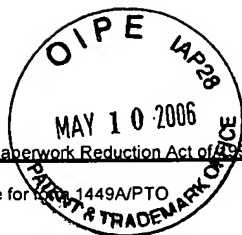
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1

of 4

Complete if Known

Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Perego
Art Unit	2188
Examiner Name	
Attorney Docket Number	RAMB-01049US2

U. S. PATENT DOCUMENTS

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		Number-Kind Code ² (if known)			
		US-5742840*	04-21-1998	Hansen et al.	
		US-5748872*	05-05-1998	Norman	
		US-5860080*	01-12-1999	James et al.	
		US-5867422*	02-02-1999	John	
		US-5898863*	04-27-1999	Ofer et al.	
		US-6006318*	12-21-1999	Hansen et al.	
		US-6034878*	03-07-2000	Osaka et al.	
		US-6038682*	03-14-2000	Norman	
		US-6092229*	07-18-2000	Boyle et al.	
		US-6125419*	09-26-2000	Umemura et al.	
		US-6151648*	11-21-2000	Haq	
		US-6154826*	11-28-2000	Wulf et al.	
		US-6160423*	12-12-2000	Haq	
		US-6255859*	07-03-2001	Haq	
		US-6263413*	07-17-2001	Motomura et al.	
		US-6327205*	12-04-2001	Haq	
		US-6408402*	06-18-2002	Norman	
		US-6487102*	11-26-2002	Halbert et al.	

FOREIGN PATENT DOCUMENTS

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Sheet 2

of 4

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Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Perego
Art Unit	2188
Examiner Name	
Attorney Docket Number	RAMB-01049US2

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		Number-Kind Code ² (if known)			
		US-6502161*	12-31-2002	Perego et al.	
		US-6513080*	01-28-2003	Haq	
		US-6154855*	11-28-2000	Norman	
		US-6345321*	02-05-2002	Litaize et al.	
		US-6369605*	04-09-2002	Bonella et al.	
		US-6449213*	09-10-2002	Dodd et al.	
		US-6625687*	09-23-2003	Halbert et al.	
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**INFORMATION DISCLOSURE
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Complete if Known

Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Perego
Art Unit	2188
Examiner Name	
Attorney Docket Number	RAMB-01049US2

Sheet 3 of 4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		*U.S. Patent Application Serial No. 10/713,868, filed 11-14-2003 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/714,025, filed 11-14-2003 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/714,026, filed 11-14-2003 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/883,474, filed 06-30-2004 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/882,999, filed 06-30-2004 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/859,438, filed 05-31-2004 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/858,850, filed 05-31-2004 by Pete D. Vogt	
		*U.S. Patent Application Serial No. 10/859,060, filed 05-31-2004 by Pete D. Vogt	
		*NG, R. (Sun Microsystems Inc.), "Fast computer memories", IEEE Spectrum, October 1992, pp. 36-39	
		*SALTERS, R.H.W. (Philips Research Laboratories), "Fast DRAMS for sharper TV", IEEE Spectrum, October 1992, pp. 40-42	

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				Application Number	10/766,131
				Filing Date	January 28, 2004
				First Named Inventor	Perego
				Art Unit	2188
				Examiner Name	
				Attorney Docket Number	RAMB-01049US2
Sheet	4	of	4		

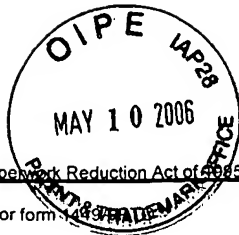
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STATEMENT BY APPLICANT**

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Sheet 1

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Application Number	10/766,131
Filing Date	January 28, 2004
First Named Inventor	Perego
Art Unit	2188
Examiner Name	
Attorney Docket Number	RAMB-01049US2

U. S. PATENT DOCUMENTS

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		Number-Kind Code ² (if known)			
		US-6425064 B2*	07-23-2002	Soderquist	
		US-4621339*	11-04-1986	Wagner et al.	
		US-4747070*	05-24-1988	Trottier et al.	
		US-4858107*	08-15-1989	Fedele	
		US-5602780*	02-11-1997	Diem et al.	
		US-5642444*	06-24-1997	Mostafavi	
		US-5838985*	11-17-1998	Ohki	
		US-6708248*	03-16-2004	Garrett, Jr., et al.	
		US-5982238*	11-09-1999	Soderquist	
		US-6639820 B1	10-28-2003	Khandekar et al.	
		US-6820163 B1	11-16-2004	McCall et al.	
		US-6553450 B1	04-22-2003	Dodd et al.	
		US-6510503	01-21-2003	Gillingham et al.	
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		EP 0 282 070 B1*	08-03-1994	Fujitsu Limited		

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				Application Number	10/766,131
				Filing Date	January 28, 2004
				First Named Inventor	Perego
				Art Unit	2188
				Examiner Name	
				Attorney Docket Number	RAMB-01049US2
Sheet	2	of	2		

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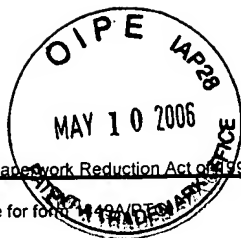
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Sheet	1	of	1
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**INFORMATION DISCLOSURE
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Sheet 1

of

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Attorney Docket Number	RAMB-01049US2

U. S. PATENT DOCUMENTS

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Complete if Known

Application Number

10/766,131

Filing Date

January 28, 2004

First Named Inventor

Perego

Art Unit

2188

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Attorney Docket Number

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

**Title of
Invention****CONFIGURABLE WIDTH BUFFERED MODULE**

Application Number: 10/766131

10/766131

Confirmation Number: 3149

First Named Applicant: Richard Perego

Attorney Docket Number: RAMB-01049US2

Art Unit: 2188

Search string: (5513377 or 6526469 or 6185654 or 6530033 or 5228132).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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	2	6526469 *	2003-02-25	Drehmel et al.			
	3	6185654 *	2001-02-06	Van Doren			
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	5	5228132 *	1993-07-13	Neal et al.			

Signature**Examiner Name****Date**

ELECTRONIC INFORMATION DISCLOSURE STATEMENT
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Electronic Version v18

Stylesheet Version v18.0

Title of Invention	CONFIGURABLE WIDTH BUFFERED MODULE
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Application Number: 10/766131

10/766131

Confirmation Number: 3149

First Named Applicant: Richard Perego

Attorney Docket Number: RAMB-01049US2

Art Unit: 2188

Search string: (6330687 or 5371880 or 5475818 or 5400360 or 4631666 or 5655113 or 5511224 or 5574945 or 5917760 or 6016282 or 6449727 or 4644532 or 4667305 or 4747100 or 4864563 or 5228134 or 5355467 or 5408646 or 5537394 or 5544342 or 5553266 or 5557266 or 5604735 or 5630095 or 5659710 or 5787083 or 5802054 or 5802565 or 5805798 or 5848145 or 5884036 or 5893921 or 5900017 or 5901294 or 5911052 or 5913044 or 5923893 or 6247100 or 20040095838 or 20040260991 or 20040250181 or 20040250153 or 20040150024 or 20040246786 or 20040246785 or 20040246767 or 20040015650 or 20030177313 or 20020083287).pn.

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Remarks

Note: Remarks are not for responding to an office action.

An Information Disclosure Statement containing 5 Foreign Patent Document and 3 Non Patent Literature Documents is being filed concurrently, via US mail. A fee for both Information Disclosure Statements is included with this submission.

Signature

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